ZC1103

A SUB-1GHz HIGHLY INTEGRATED WIRELESS TRANSCEIVER

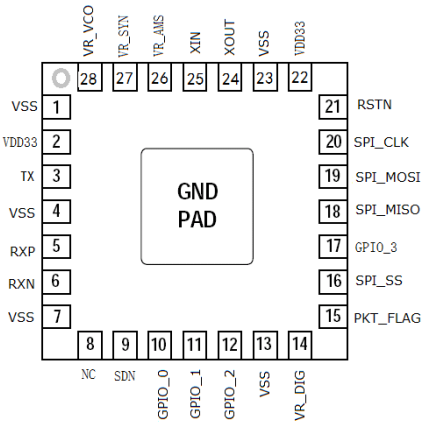
Features

- Frequency
  - range = 200 to 1000MHz
  - Support for 230/315/408/433/868/915MHz band
- Receiver sensitivity = -112Bm@ 10Kbps
- Max output power
  - +20dbm
- Modulation
  - FSK
  - GFSK
- Data rate = 2.4kbps to 200kbps
- Support for SPI interface
- Auto-answer & auto-retransmission
- Fast channel hopping
  - Support for frequency hopping algorithm
- Support for RSSI
- Antenna diversity and T/R switch control
- Automatic frequency control (AFC)
- Automatic gain control (AGC)
- Low operating voltage = 1.9V to 3.6V
- 28-Pin QFN 5*5 package

SRT is our wireless communication brand

Applications

- SRT DALI light control
- SRT Power Supply
- wireless sensor
- SRT CO2 sensor
- SRT Temperature sensor
- SRT Humidity sensor
- SRT terminor
- SRT gateway
- Smart meters
- Industrial sensors & wireless industrial control equipment
- Wireless gaming devices
- Remote sensing
- Security & protection system
- Smart fitness equipment
- Smart TV controllers
- Wireless sensor tags
- Wireless door security
- Smart Agriculture
- Remote controllers
- Wireless toys



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1. Introduction

The ZC1103 is an integrated single-chip radio transceiver designed for high-performance at low-power and low-voltage operation. The ZC1103 covers a frequency range of 470Hz - 510Hz, as well as an ISM frequency band at 433MHz. The ZC1103 integrates functional blocks including an RF receiver, an RF transmitter, a frequency synthesizer, a GFSK modulator, a GFSK demodulator, etc. The ZC1103 provides a flexible configuration of output power, channel selection, and packet format through SPI interfaces that are equipped with built-in CRC, FEC, and auto-answer & auto-retransmission mechanisms, which greatly simplifies system design and optimizes performance.

The ZC1103 operates as a time division duplexing (TDD) transceiver, meaning the device transmits and receives data packets alternately at different times. The ZC1103 converts the received (G)FSK modulated signals to IF frequency through a frequency mixer, and then feeds these signals to the subsequent IF filter and variable gain amplifier (PGA) for filtering and amplification. The processed IF signals are converted to the digital domain by a high-performance sigma-delta ADC while the built-in DSP performs functions such as filtering, demodulation, automatic gain control, RSSI detection, packet processing, etc.

The high-precision local oscillator (LO) inside the ZC1103 is achieved by implementing a sigma-delta Fractional-N frequency synthesizer and can be used for both receiving and transmitting. The transmitted FSK data are modulated directly into the sigma-delta stream and can be filtered by the internal Gaussian filter to reduce excess spectral components.

The ZC1103’ s internal high-efficiency Class E power amplifier (PA) consumes about 100mA of current at +20dBm of output power. The output power of the PA can be set between -5dBm and +20dBm with a 1dB accuracy. The PA turn-on time can be controlled by an internal auto-tilt rise curve to minimize interference with other modules on the device as well as to reduce excess spectrum expansion.

The ZC1103 supports TX/RX switch control and antenna diversity switch control

to extend the link range and improve performance. A low-power 32KHz oscillator is integrated into the device, enabling automatic wake-up with reduced overall current consumption.

2. Absolute Maximum Ratings

Table 1. Absolute maximum ratings

PARAMETER		MIN	MAX	UNIT
Operating temperature	Top	-40	100	℃
Storage temperature	Tstor	-55	125	℃
Supply voltage	VDD	-0.3	3.7	V
Input RF level	Pin_max		+10	dBm
ESD(Human-body model)	ESD_HBM		2	KV

* Caution: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device.

* Caution: The ZC1103 is an electrostatic-sensitive device, please follow a guide when handling it.

3. Electrical Specifications

Table 2. ZC1103 electrical specifications

Symbol	Conditions (unless otherwise stated, VCC = 3.3V, TA=25℃)	Parameters			Units
		Min	Typ	Max	
Operating Conditions					
VDD	Supply voltage	1.9	3.3	3.6	V
VSS	Ground		0		V
V_{OH}	High-level output voltage	VDD-0.3		VDD	V
V_{OL}	Low-level output voltage	VSS		VSS+0.3	V
V_{IH}	High-level input voltage	2.0	3	3.6	V
V_{IL}	Low-level input voltage	VSS		VSS+0.3	V
Cin	Input capacitance			10	pF
	Operating temperature	-40		+85	℃
	Storage temperature	-40		+125	℃
Current Consumption					
ICC	Shutdown state		0.1		uA
	Standby state		3		uA
	IDLE state		1.3		mA
	TX state (20dBm)		100		mA
	TX state (7dBm)		36		
	TX state (0dBm)		25		
	RX state		18		mA
	RX state (wor)		3		mA
General Conditions					
f_{OP}	Operating frequency	420		520	MHz
f_{XTAL}	Crystal frequency	16	18.08	28	MHz
PLL_stable	PLL stable time		250		us
	Data rate	2.4		200	kbps
Transmitter Operation					
P_{MAX}	Maximum output power		20		dBm
PRFC	Power control range	-5		20	dBm
P_{STEP}	Power control step		1		dB

Receiver Operation					
RXSENSE	Receiver sensitivity (0.1%BER@10kbps)		-112		dBm
Anti-interference Characteristics					
C/I_{CO}	Co-channel interference		9		dBc
C/I_{1ST}	1st adjacent-channel interference		-44		dBc
C/I_{2ND}	2nd adjacent-channel interference		-52		dBc
C/I_{3RD}	3rd adjacent-channel interference		-60		dBc

4 Functional Block Diagram

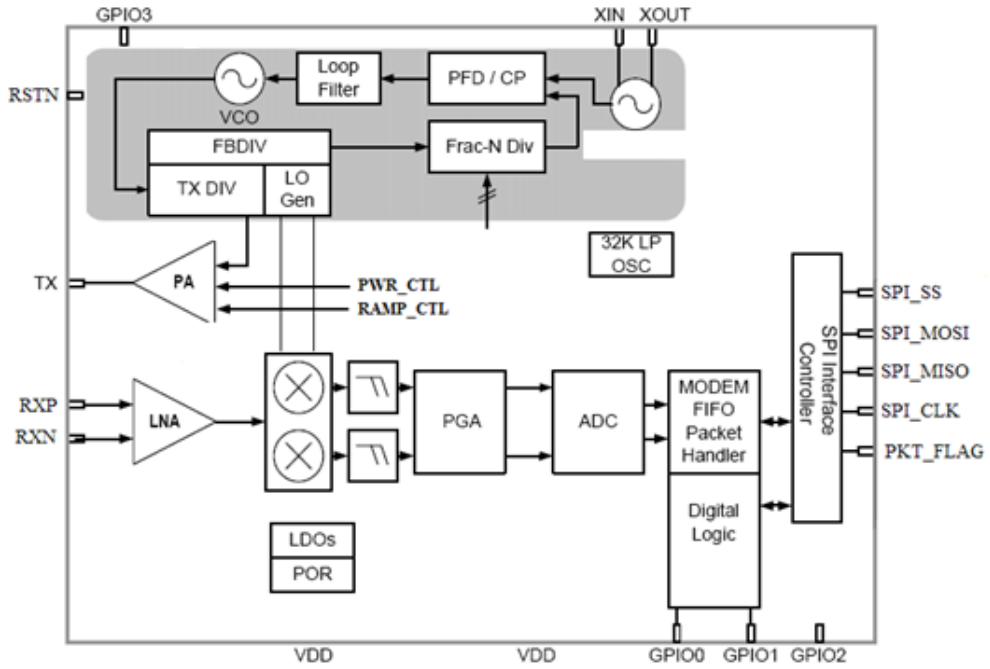


Figure 1. ZC1103 block diagram

5. Pin Information

5.1. Pin Assignment

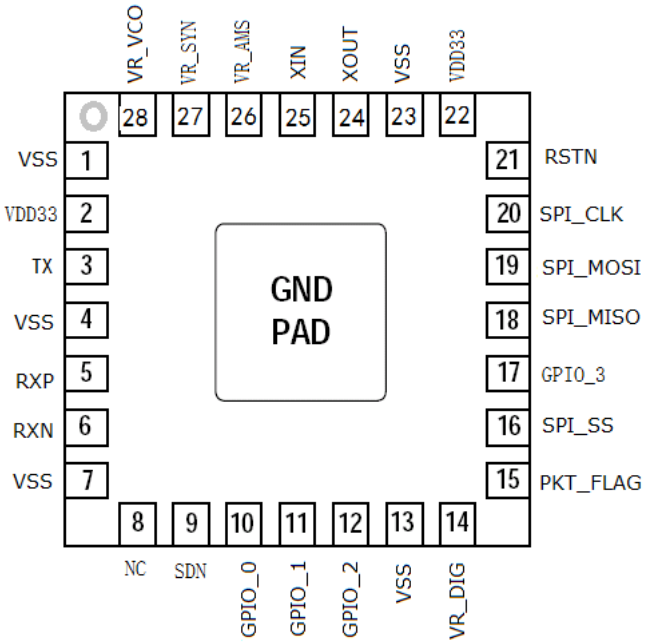


Figure 2. ZC1103 pin assignment (top view) for the QFN 28 5*5 package

5.2 Pin Functions

Table 3. ZC1103 pin functions

Pin	Pin Name	Type	Description
1	VSS	GND	Ground connection
2	VDD33	VDD	1.9V - 3.6V power supply
3	TX	RF O	PA open-drain output, with external LC matching network
4	VSS	GND	Ground connection
5	RXP	RF I	Differential RF input
6	RXN	RF I	
7	VSS	GND	Ground connection
8	NC	NC	Not connected
9	SDN	DI	Shutdown control input, active-high

10	GPIO_0	DO	General-purpose Output
11	GPIO_1	DO	
12	GPIO_2	DO	
13	VSS	GND	Ground connection
14	VR_DIG	VDD	1.8 V power supply output for LDO regulator of internal digital block
15	PKT_FLAG	DO	Transmit/receive packet status indicator bit
16	SPI_SS	DI	Enable SPI input, active-low. Also used to bring the device out of sleep mode
17	GPIO_3	DO	General-purpose Output
18	SPI_MISO	DO	SPI slave data output
19	SPI_MOSI	DI	SPI slave data input
20	SPI_CLK	DI	SPI clock input
21	RST_N	DI	Asynchronous, active-low digital reset
22	VDD33	VDD	1.9V - 3.6V power supply
23	VSS	GND	Ground connection
24	XOUT	AO	Crystal oscillator output
25	XI	AI	Crystal oscillator input
26	VR_AMS	VDD	1.8 V power supply output for LDO regulator of internal SYN block
27	VR_SYN	VDD	1.8 V power supply output for LDO regulator of internal AMS block
28	VR_VCO	VDD	1.8 V power supply output for LDO regulator of internal AMS block
PKG	PAD_GND	GND	Ground connection

6. Serial Peripheral Interface (SPI)

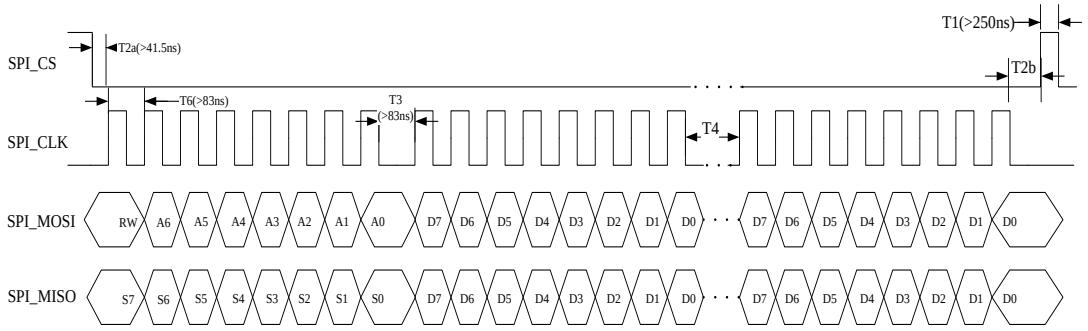
All of the function control of ZC1103 is under SPI command. The clock polarity of the SPI is positive, and the clock phase of the SPI is selectable. When ckpha=1, data are sampled on the falling edges; when ckpha=0, data are sampled on the rising edges.

The internal blocks are accessed by the device via SPI read and write registers. The SPI R/W data is in byte format. When accessing the address corresponding to FIFO, the SPI controller will automatically add the FIFO address if accessing consecutively in bytes within one SPI_CS cycle.

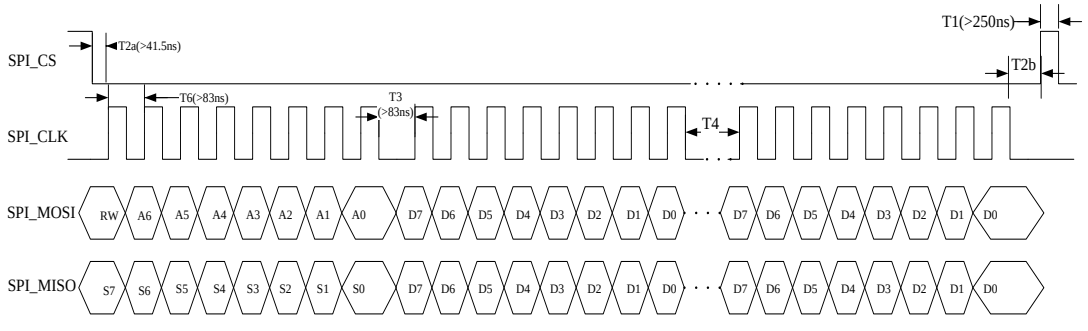
When there is no external crystal frequency, SPI cannot write data, but it can still read registers' data.

Figures 3 , 4. SPI Timing Diagram

When ckpha=1, sampling on the falling edges



When ckpha=0, sampling on the rising edges



CKPHA=0

Note:

1. SPI W/R bit: Write = 0, Read = 1
2. The device will automatically add the register address when SPI read and write

multiple consecutive registers in one SPI_CS cycle.

Table 3. SPI Timing Requirements

Name	Min	Typ	Max	Description
T1	250ns			Time between two SPI visits
T2a,T2b	41.5ns			Time between SPI_CS and SPI_CLK
T3	Note1			Time between address and data
T4	Note2			Time between to register data
T6	83ns			Time for one SPI_CLK clock cycle

Notes:

1. The device needs 450ns to find the correct FIFO pointer address before accessing the FIFO data.
2. The device needs to wait at least 450ns before reading the FIFO data. When reading other registers, T4min = 41.5ns.

7. State Machine Diagram and Operational Modes

7.1 State Machine Diagram

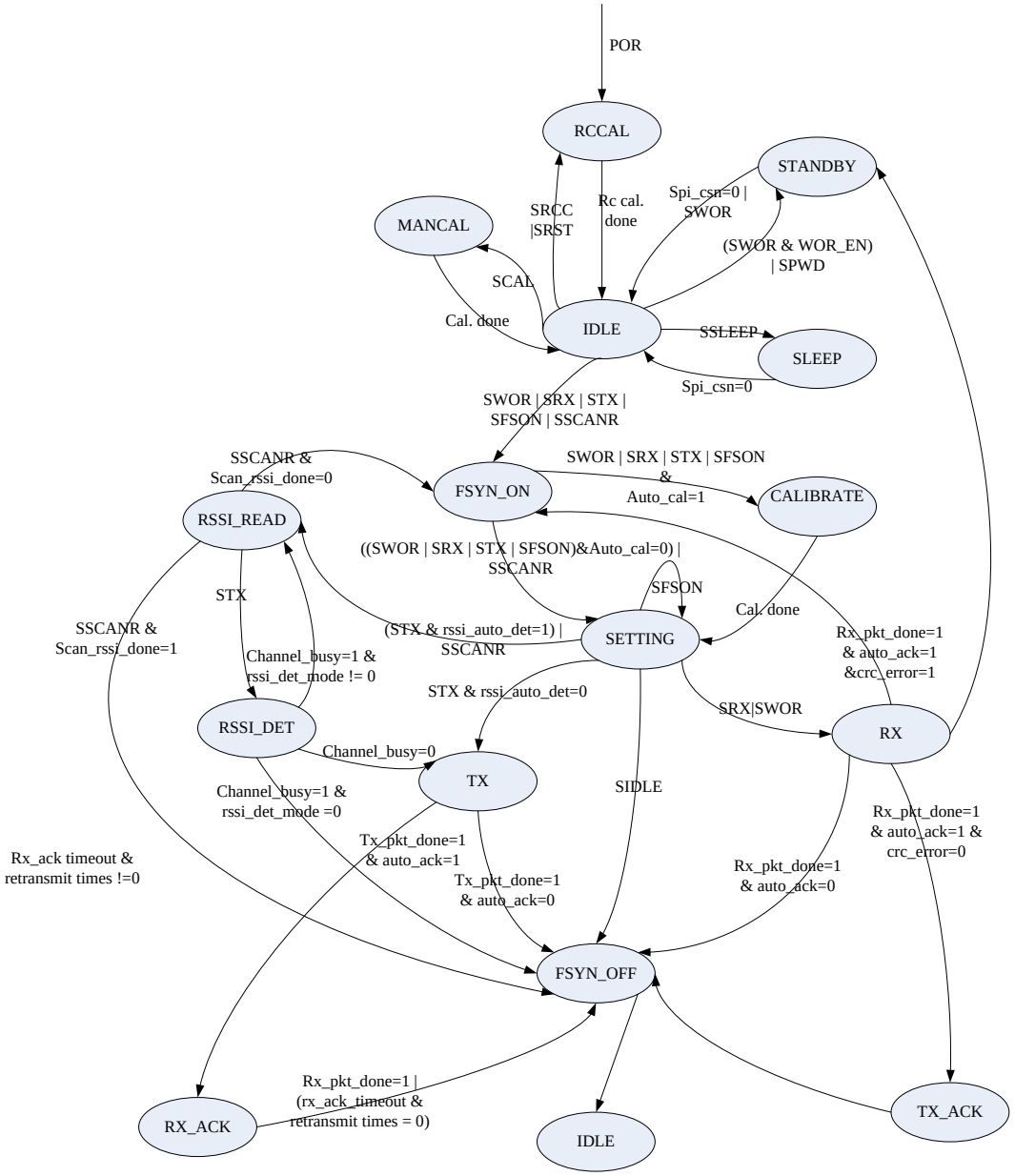


Figure 5. State-transition diagram

7.2 Operational Modes

Table 4. Main operational modes (shutdown state not included)

State/mode	Description	Command	Transit Time
IDLE State	Idle state. Entering the state by resets.	SIDLE	
SLEEP state	Sleep state. The lowest current consumption state other than STANDBY state.	SSLEEP	SLEEP=>IDLE 2ms
STANDBY state	Standby state. The lowest current consumption state.	SPWD/SWOR	STANDBY=>IDLE 2ms
FSON state	Frequency synthesizer opened state. Enable to switch to RX state or TX state quickly.	SFSON	FSON => RX Less than 5us
RX state	Data receiving state.	SRX	IDLE=>RX Less than 250us
TX state	Data transmitting state.	STX	IDLE=>TX Less than 250us

1、Shutdown State

When SDN gets high-level inputs, the device enters shutdown state. All internal circuit of the device enters shutdown state with a current consumption of 100nA.

2、IDLE State

After resetting or sending a SIDLE command, the device enters IDLE state to wait for a command from SPI interface to perform another action.

3、 SLEEP State

After receiving a SSLEEP command, FSM enters SLEEP state. In SLEEP state, the external crystal frequency is shut down while digital power is on. The current consumption is low in SLEEP state. To wake up from SLEEP state, set the SPI_CSN bit to 0.

4、STANDBY State

After receiving a SWOR command while enabling the WOR function, or after receiving a SPWD command, the device enters STANDBY state. In STANDBY state, the power supply and external crystal frequency are turned off to enter a low current consumption state while the registers' data is retained. To wake up from STANDBY state to IDLE state, set the SPI_CSN bit to 0 or trigger a SWOR event.

5、FSON State

Please hold FSON state after opening the frequency synthesizer. In FSON state, the device will get into TX/RX state immediately when receiving a TX/RX command.

6、TX State

After receiving a TX packet command, the device will first open PLL and VCO to calibrate and wait until it reaches the PPL-required transmitting frequency band. When automatic channel detection is running, the RSSI value of the channel is read before entering TX mode. If the channel is free, the packet will transmit; if the channel is busy, then the next action can be set through the register by deciding whether to quit transmission or to continue detecting RSSI value until the packet is sent.

After transmitting the packet, the state machine will switch to RX_ACK state to make sure the packet is received correctly by the receiver if the auto-answer function is open. If the receiver does not receive the packet within the time limit set by the register, the device will retransmit the packet. The maximum number of retransmissions can be set through the register.

7、 RX State

After a receiving RX packet command, the device will first open PLL and VCO to calibrate and wait until it reaches the PPL-required transmitting frequency band,

then open the receiver circuit (LNA, frequency mixer, and ADC), and finally open the RX state of the digital modem until it receives a data packet completed indication signal or a SWOR function time-out signal. When the device receives a SWOR function time-out signal, the state machine enters STANDBY; when it receives a data packet completion indication signal, the device transmits the ACK packet and enters IDLE state if the AUTO_ACK function is open.

8、Interrupts

The device can generate two interrupts: pkg_flag and fifo_flag (configured through GPIO_1). These two interrupt flags are readable. The pkt_flag contains 4 functions: preamble matching, syncword matching, receive packet completion and transmit packet completion. When pkt_length_e = 1 (packet length is the first byte of payload), pkg_flag can be set to sycnword matching or packet completion state, packet completion is the default. When pkt_length_en=0, pkg_flag indicates preamble matching or syncword matching and denotes packet completion in TX state.

Fifo_flag indicates whether or not the FIFO is full: FIFO is empty in TX state; FIFO is full in RX state.

8. Functional Blocks Description

The following sections demonstrate the key internal blocks and features.

8.1 Frequency Synthesizer

Precise carrier waves are generated by the internal frequency synthesizer of the device. There are two methods for configuring channel frequency:

1) Choose a frequency value from a list of channel-group numbers.

2) Calculate the frequency value using the register setting. The calculation formula is as follows:

f=f0+N*step

N={reg0[6:0]};

step={reg1,reg2,reg3}，the low 20-bit is used to represent fractional numbers;

f0={reg74,reg75,reg76,reg77}, the low 20-bit is used to represent fractional numbers, the unit is MHz;

Then, check whether the state machine is in RX state or TX state. If it is in RX state, add or subtract a frequency offset value of medium frequency.

Reference frequency can also be set through the register. The default value is 16M, ref_freq= {reg70[6:0], reg71, reg72, reg73}, and the low 24-bit is used to represent fractional numbers. The deviation of different crystal oscillators can be offset by setting the reference frequency.

8.2 Automatic Gain Control (AGC)

The signal peak detector for ADC can apply optimal tuning for LNA gain and PGA gain to reach the best performance.

8.3 Received Signal Strength Indicator (RSSI)

RSSI is used to estimate the signal strength in the receiver’ s interval channel. The RSSI estimation must be taken in RX state so that the RSSI value can be read by register directly.

8.4 Automatic frequency control (AFC)

The frequency detuning caused by the uncertainties of crystals can be compensated by opening the digital AFC in RX state. When AFC is running, the length of the preamble should be long enough to stabilize AFC.

8.5 Data Processing

1. RX FIFO and TX FIFO

There are two FIFOs in the device. Both FIFOs have 128 bytes available for transmitting or receiving data. These two FIFOs can be combined into one FIFO by setting the register, with 256 bytes for both transmitting and receiving. When transmitting or receiving, the read and write pointers of this FIFO are still controlled separately. TX FIFO and RX FIFO can both set a threshold via the register. When the threshold is triggered, the FIFO_FLAG signal is generated.

Under TX state, when the data in TX FIFO reach the threshold, the FIFO_FLAG signal appears. But if there is more data to be written into TX FIFO, causing the data in TX FIFO to be larger than it should be, the FIFO_FLAG will be cleared automatically. Under RX state, the FIFO_FLAG also appears when the received data reach the threshold. In case the FIFO overflows, the MCU should read data from RX FIFO at this time.

The read and write pointers of RX and TX can be zeroed by writing 1 to their corresponding register.

The RX writing pointer will be auto-zeroed when starts to receive a data frame.

The TX reading pointer will be auto-zeroed when starts to transmit a data frame.

2. Data mode

(a). FIFO data mode

The data that need to send by MCU are written to TX FIFO through the SPI interface, which automatically packages the FIFO data when transmitting. The data inside the FIFO is only written in the payload section. Under FIFO mode, there are several scenarios:

Table 5. Different situations under FIFO mode

	pkt_length_en	hw_fw_en					
1	1	x	preamble	syncword	payload length	payload	crc
			1-255bytes	1-4bytes	1/2bytes	N bytes	2bytes
2	0	1	preamble	syncword	payload		
			1-255bytes	1-4bytes	N bytes		
3	0	0	preamble	syncword	Payload		
			1-255bytes	1-4bytes	N bytes		

1) In the first method, the length of the payload is controlled by the first byte or WORD in the payload. When the transmitting data arrives, the state machine will exit to IDLE state by itself, and both the preamble and the syncword will be added automatically. CRC can do self-calculation and place itself at the end of the data. This method is the most commonly used

2) In the second method, the payload does not contain data length. The state machine will exit to IDLE state when transmitting FIFO is empty. Whether to add a preamble and syncword can be set via the register when transmitting.

3) In the third method, the payload does not contain data length. At the same time, the transmission does not stop when the transmitting FIFO is empty. To exit and enter IDLE state, a SIDLE command should be sent by MCU. Whether to add a preamble and syncword can be set via the register when transmitting.

The preamble sequence is 0101....0101 or 1010....1010.

Syncwords can be set through the register.

Except for preambles, all data from other sections are sent by low bit first.

Data in the payload support data whitening, FEC, and interleaving.

(b). Direct mode

In direct mode, the RX or TX data does not go through the FIFO and packet processing system and is directly inputted or outputted to serial data through pins.

8.6 Wake-up Timer

The device contains an integrated wake-up timer that can wake up the device

from STANDBY state periodically. The wake-up timer runs with an internal 32K clock source.

The timer can be used to set the time the device sleeps and wakes up to execute commands. To configure them, set the timer's clock source to a 2^(015) division 32K clock. The command that is executed after waking up can be set to RX or TX.

The counter can be configured with a maximum value wortimer_set and an intermediate value wor_rxtimer_set, which can easily generate a PWM-like signal output. Wortimer_set sets the entire one cycle time, whereas wor_rxtimer_set sets the receiving time after wake-up.

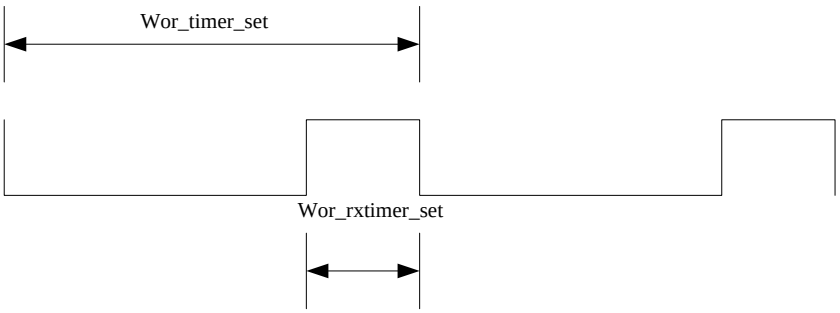


Figure 5. Counter timing diagram

When a valid packet is received, the device will exit the auto-wakeup state and generates a PKT_FLAG signal to notify the MCU to process the data.

9. Typical Application Circuit

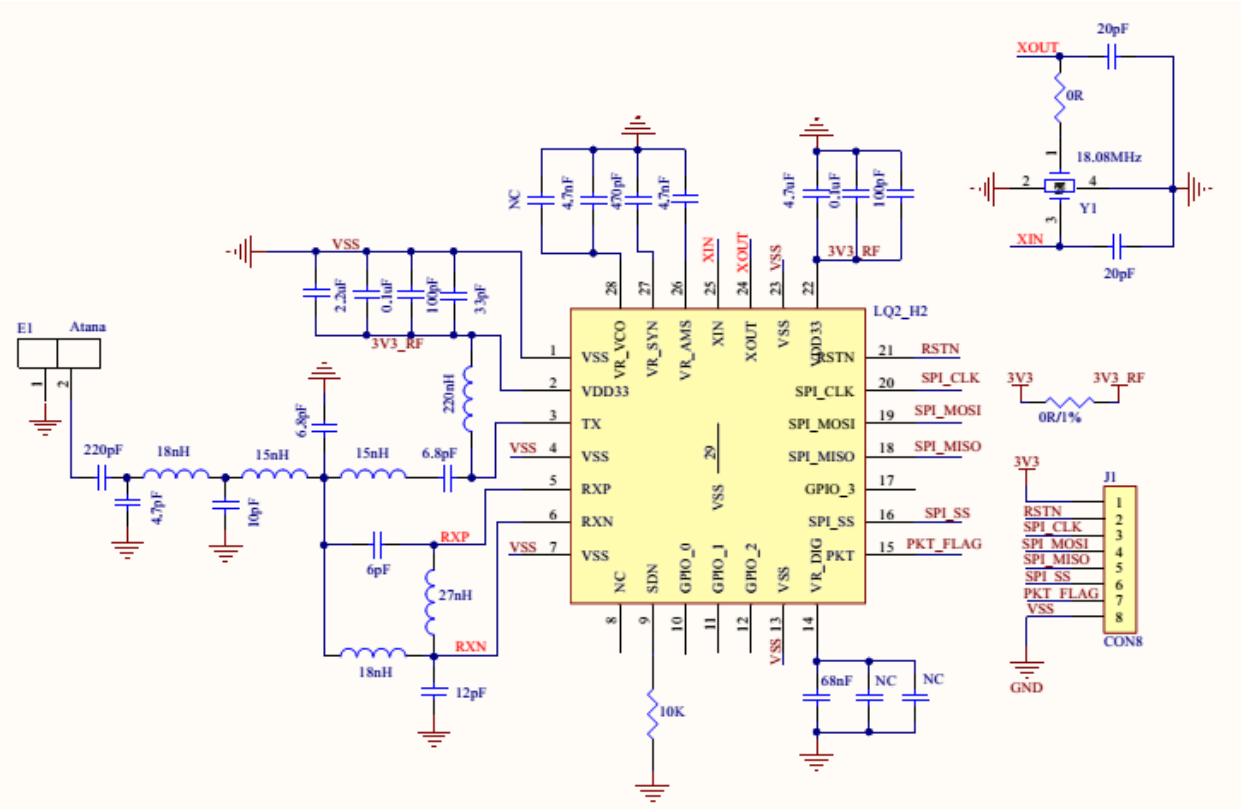


Figure 6. A typical application circuit at 480MHz band

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